Dolendra Vikas Addepalli

+1 (213) 247-0066 | daddepal@usc.edu | linkedin.com/in/dolendravikas/ | GitHub | vikky.netlify.app

Education

University of Southern California — Los Angeles, CA

Honours, Master of Science in Electrical Engineering, **GPA - 4.0/4.0** — Aug. 2023 – May. 2025

- EE577a&b VLSI System Design, EE658 Design for Testability, EE457 Computer System Organisation

Indian Institute of Information Technology, D&M, Kancheepuram — Chennai, India

Honours, B.Tech in Electronics and Communication Engineering, **CGPA - 3.82/4.0** — Jul. 2019 – May. 2023

Technical Proficiency

Programming : Verilog, C, C++, System Verilog, Python, TCL Scripting
Tools : Cadence (Innovus, Virtuoso, Calibre), Synopsys (Design Compiler, Prime Time), Vivado, Modelsim LTspice, NGSpice, KiCad, Altium, Keil uVision, MATLAB, Git
Concepts : PDN, EMIR, CTS, PnR, DFT, MBIST, Scan Chain, CDC, Synchronizers
Protocols : PCIe Gen3/Gen4, AXI, DDR3, UART
Certifications : RTL-to-GDSII Flow (by cadence), Innovus Implementation System (by Cadence), Basic Static Timing Analysis (by Cadence)

Projects

RTL to GDSII multi core NoC design | *RTL, Synthesis, STA, PnR, CTS* — Mar. 2023

- Designed a 4-stage pipeline processor with 6-stage pipeline ALU for DIV and SQRT inst' to meet timing
- Built a router that sits on top of processor and implemented XY routing algorithm to overcome deadlocks
- Parameterized the implementation to scale the NoC to 16-core and connected them in a mesh architecture
- Synthesised the netlist at 4ns and performed endpoint slack analysis using prime time
- Floorplanned the design, conducted pre-CTS timing, optimized timing and performed CTS

Processor synthesis flow with DFT | *Scan Insertion, DFT Synthesis* — Feb. 2023

- Modified the RTL by adding additional input and output ports to incorporate the scan chain
- Implemented scan chain with Muxed-D scan cells during synthesis and automated the synthesis process
- Replaced the gated clock architecture with its test equivalent architecture to increase the testability
- Created test vectors using TetraMax to check all stuck-at fault. Achieved fault coverage of 93.58%

Physical Implementation of DTMF chip | *Innovus, PnR, CTS* — Dec. 2023

- Floorplanned the design using gate-level netlist and created power rails using SRoute(Special Route)
- Analyzed the congestion using the Early Global Router to assess the design's routing capability
- Conducted pre-CTS timing analysis, optimized timing, and performed Clock Tree Synthesis using CCOpt

512-bit SRAM Macro | *Cadence Virtuoso (45nm PDK), VLSI Design* — Oct. 2023

- Designed 6T-SRAM, Row Decoder, Column Mux, Sense Amplifier, and Write Driver circuit's and layouts
- Optimized sub-circuits by implementing logic-sharing and sizing MOSFETs to minimize associated delays
- Created Python script for testing diverse-sized SRAM arrays with multiple read and write cycles
- Performed PPA analysis. Layout area = 9.6 nm^2, Max. Freq. = 1GHz, Power = 240pW/one write-read

Single Cycle CPU | *Verilog, Vivado, Micro Architecture* — Sep. 2023

- Built a 32-bit RISC processor design using verilog by implementing MIPS instructions
- Implemented R-type, I-type, and J-type instructions like LW, SW, Addi, BEQ, J, JAL, JR
- Verified individual instruction with custom testbench on vivado

Previous Internship

Hardware Design Intern — Mar. 2023 – May. 2023

Aerospace Engineers Private Limited — Salem, India

- Designed a 4-layer vehicle control board with on board jetson nano system-on-module, and multiple daughter cards
- Engineered module on/off logic and various sub-circuits that power jetson and support external peripherals
- Developed a BMS for underwater vehicle that can supply 3 voltage levels to various vehicle subsystems

Electronics Research Intern — May. 2022 – Oct. 2022

UTSAAH Lab, Indian Institute of Science, Bangalore | Certificate — Bangalore, India

- Devised analog front-end to produce constant alternating current. Achieved a correlation of 0.87
- Utilised digiPOT to control amplification factor of op-amp. Bootstrapped op-amps to double the performance
- Developed libraries for digiPOT, signal generator and written firmware to control over wi-fi